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MS-7505 ATX

Version: 0A

CPU: Intel Pentium 4 Cedar Mill / Prescott , Pentium D Smithfield / Presler and Conroe / Kentsfield family processors in LGA775 Package.

System Chipset:

NVIDIA MCP73

On Board Device:

BIOS -- SPI Flash 8M
Azalia Codec -- ALC888
LPC Super I/O -- FINTEK F71882FG
LAN -- Realtek RTL8211BL-GR
CLOCK Gen -- Integrated in MCP73
1394 Controller -- JMB381

Main Memory:

SINGLE-channel DDR-II * 4 (Max 4GB)

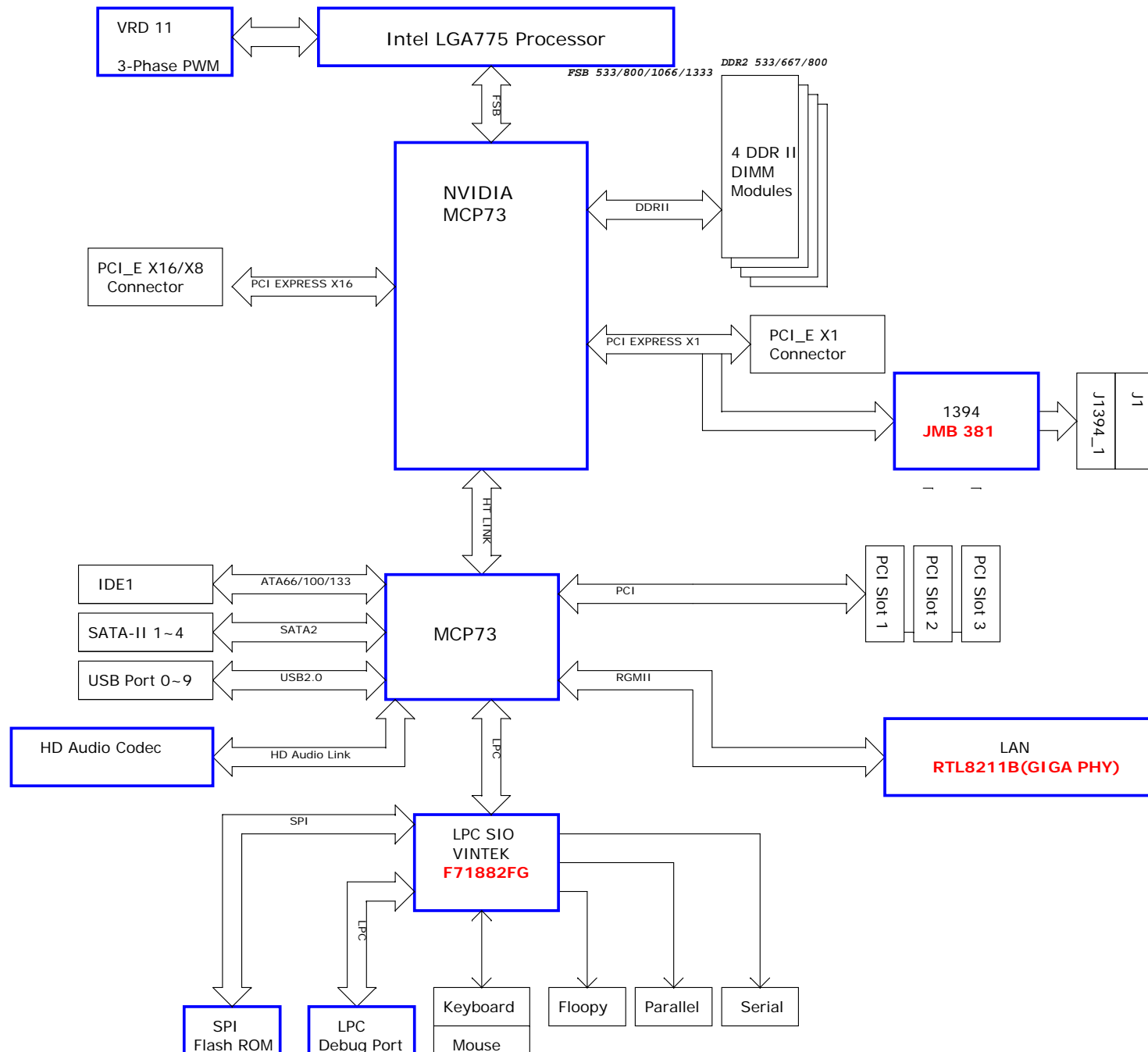
Expansion Slots:

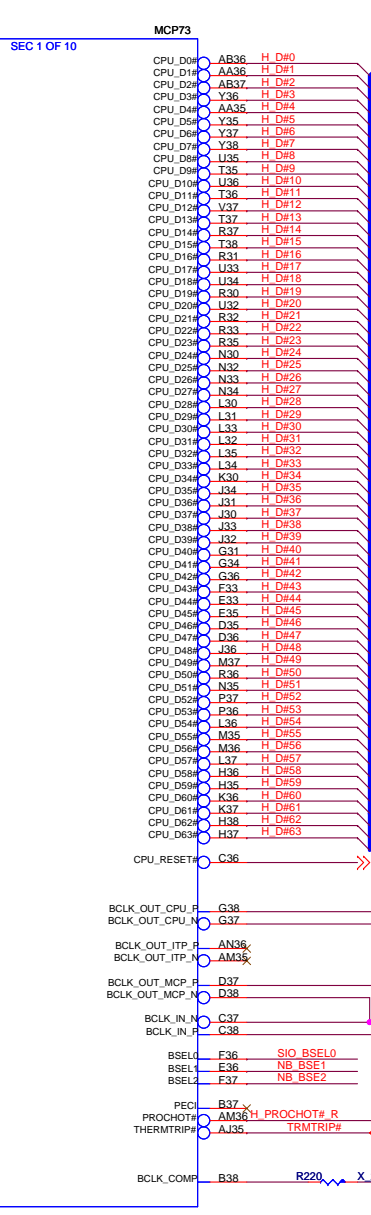
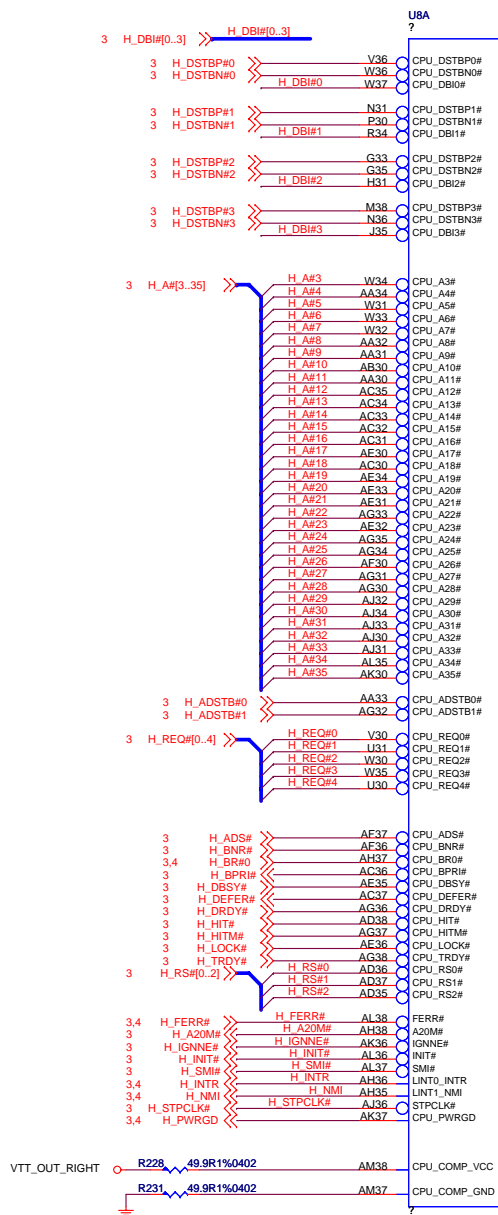
PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT * 1
PCI SLOT * 4

Intersil PWM

OPT	Function	Orcad Configure	BOM
PV	MCP73PV (HDMI+DVI) / F71882FG/ALC888/RTL8211BL/JMB381	cfg-7505-PV	601-7505-A10

Block Diagram





J1 Plug 1--2 J2 Plug 1--2 normal

400-->333 J1 Plug 2--3 J2 Plug 1--2

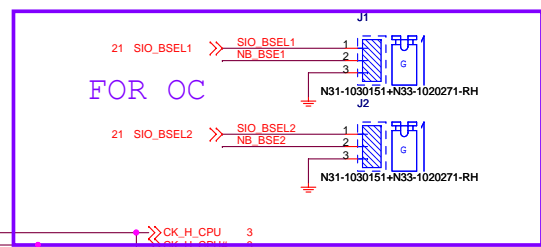
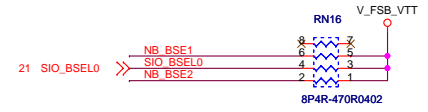
266-->333 J1 Plug 1--2 J2 unPlug

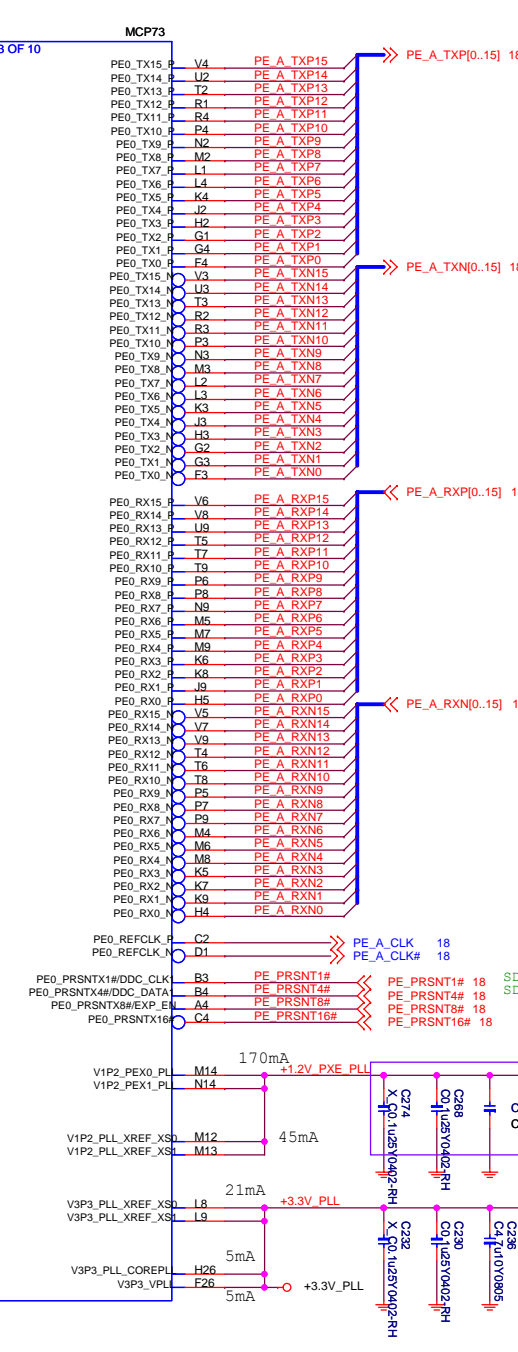
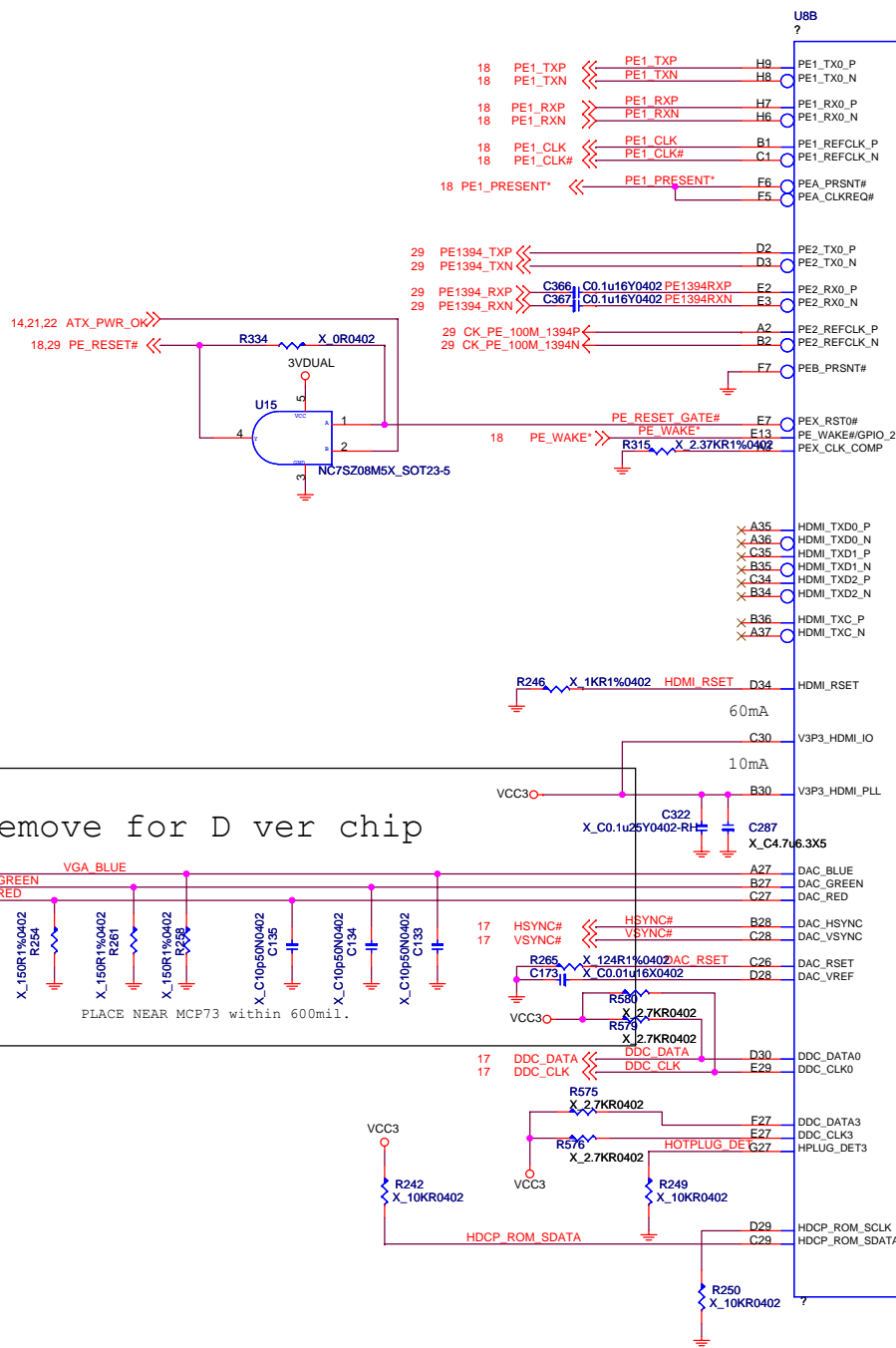
333-->266 J1 Plug 1--2 J2 Plug 2--3

400-->266 J1 Plug 2--3 J2 Plug 2--3

200-->266 J1 Plug 2--3 J2 Plug 1--2

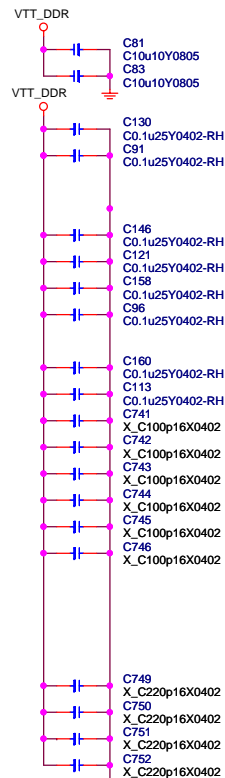
BSEL[2..0]	FSB CLK (MHz)
000	266MHz
010	200MHz
100	333MHz
TBD	Reserved



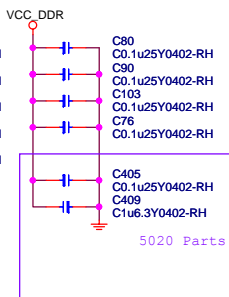
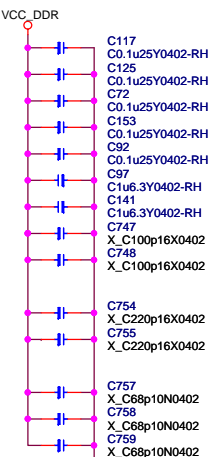
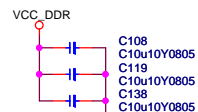
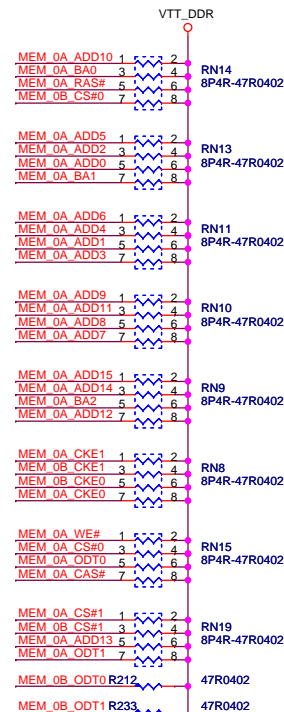
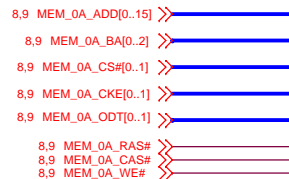


SDVO Muxing on X16 PCI Express		
PE_PRSNT1#		SDVO_SCL#
	PE_PRSNT4#	SDVO_SDA#
PE_A_TX3	PE_A_TX12	SDVO_CLK#
PE_A_TX2	PE_A_TX13	SDVO_BLUE
PE_A_TX1	PE_A_TX14	SDVO_GREEN
PE_A_TX0	PE_A_TX15	SDVO_RED
PE_A_RX1	PE_A_RX14	SDVO_INTR
PE_A_RX0	PE_A_RX15	SDVO_TVCLKIN

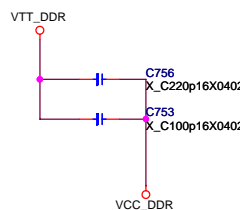
CHANNEL A VTT_DDR DECOUPLING CAPS



CHANNEL A ----- 0A , 0B



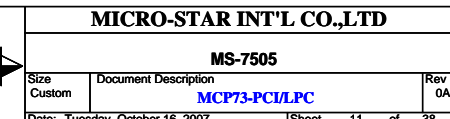
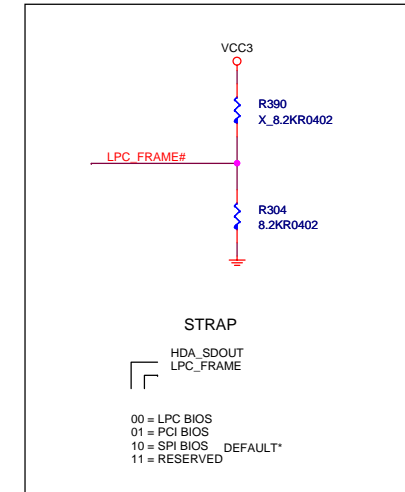
Demo Board with 0.1u X5, 1uX3, 10uX3 for Single Channel
Dual Channel Must x2

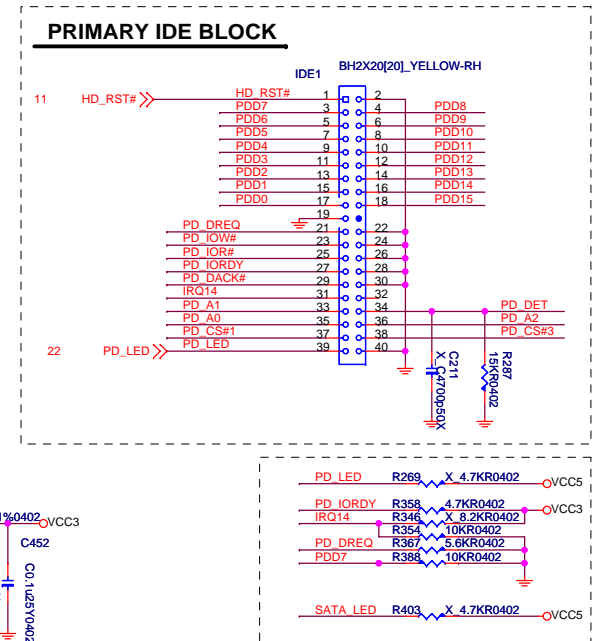
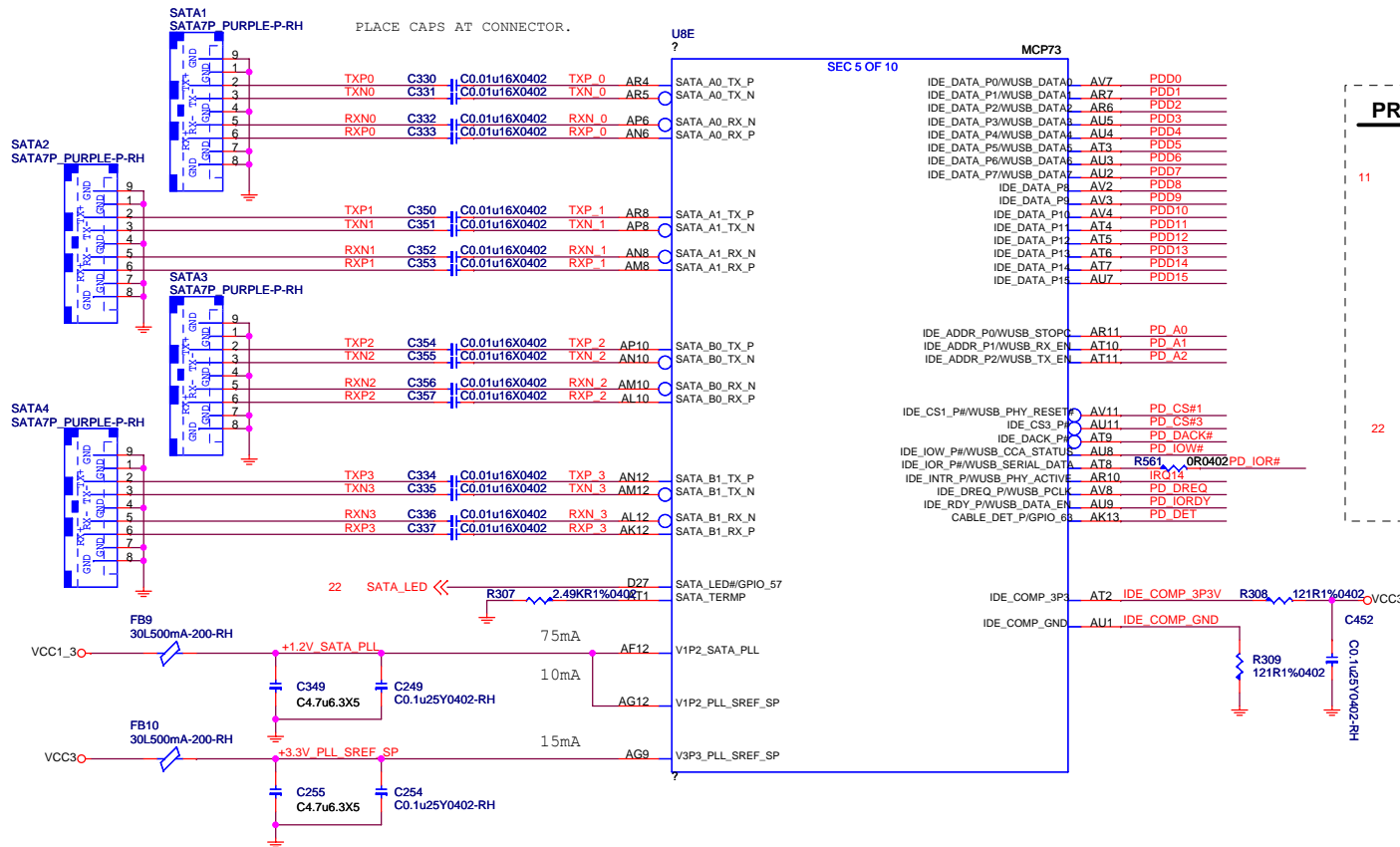


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Size	Document Description	Rev
Custom	DDR II VTT Termination & Decoupling	0A
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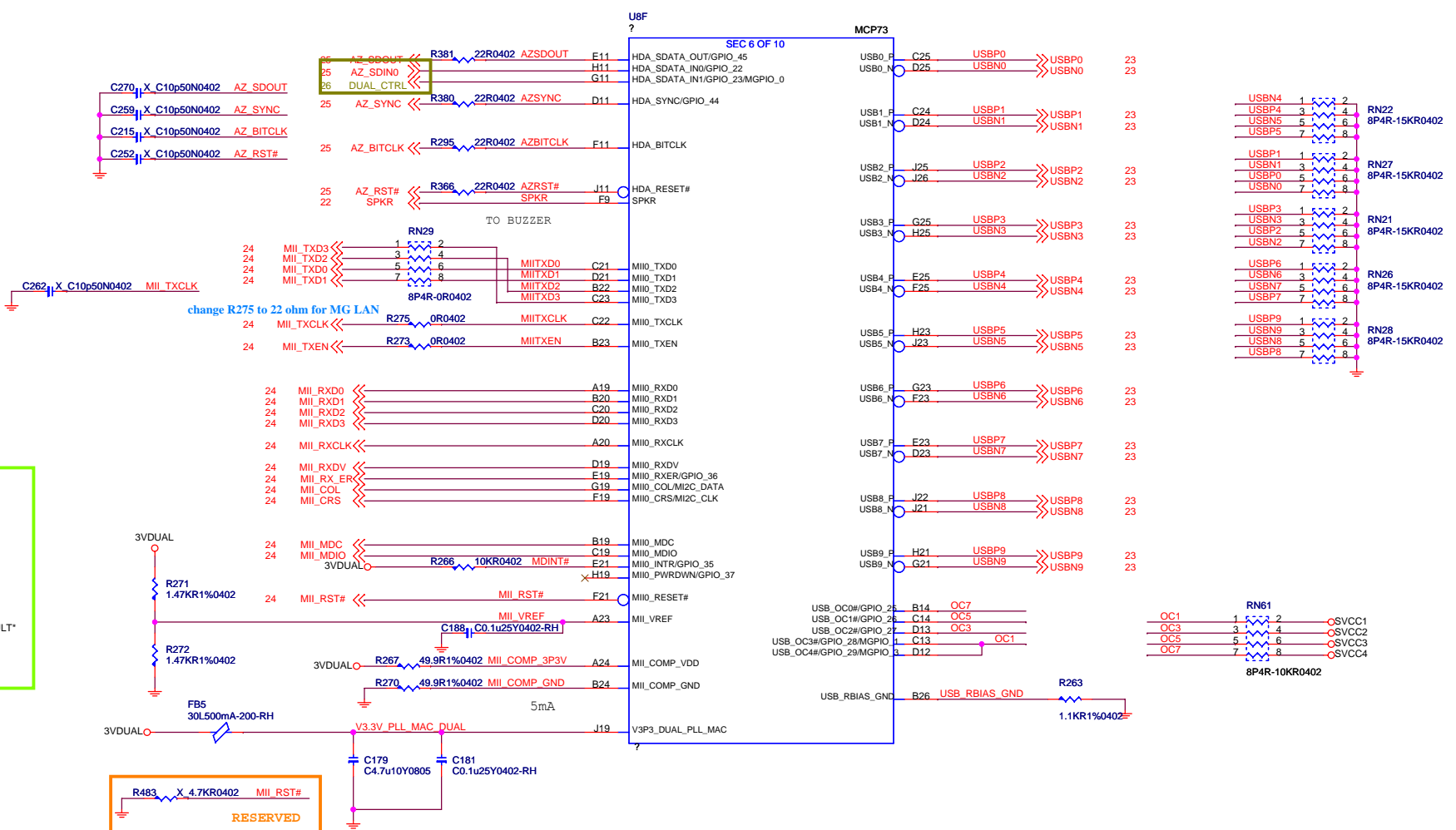
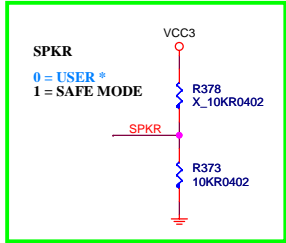
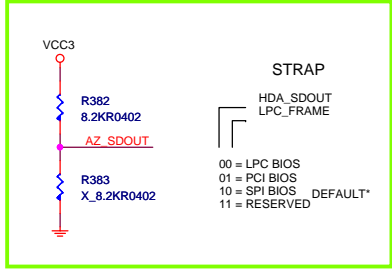
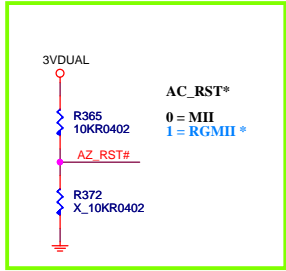
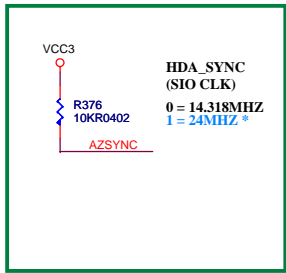




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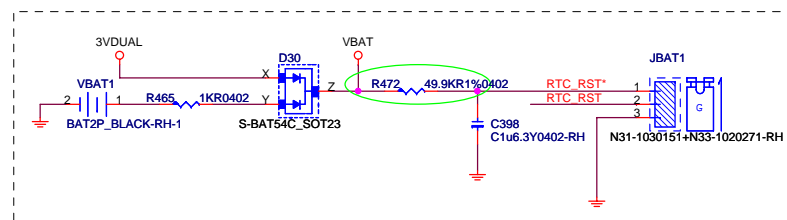
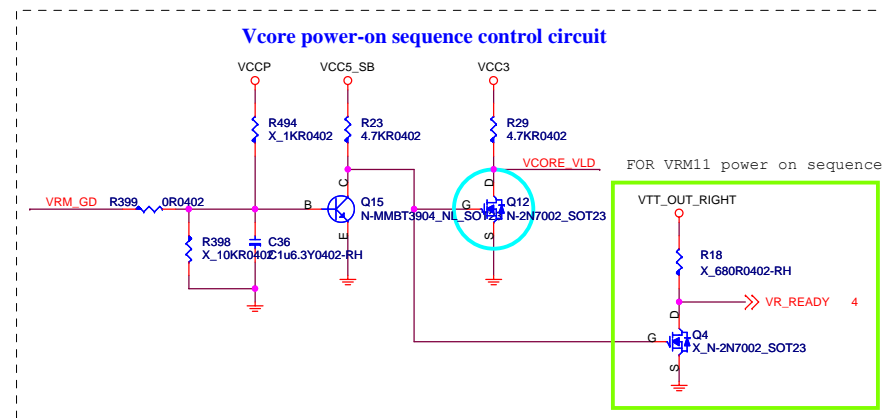
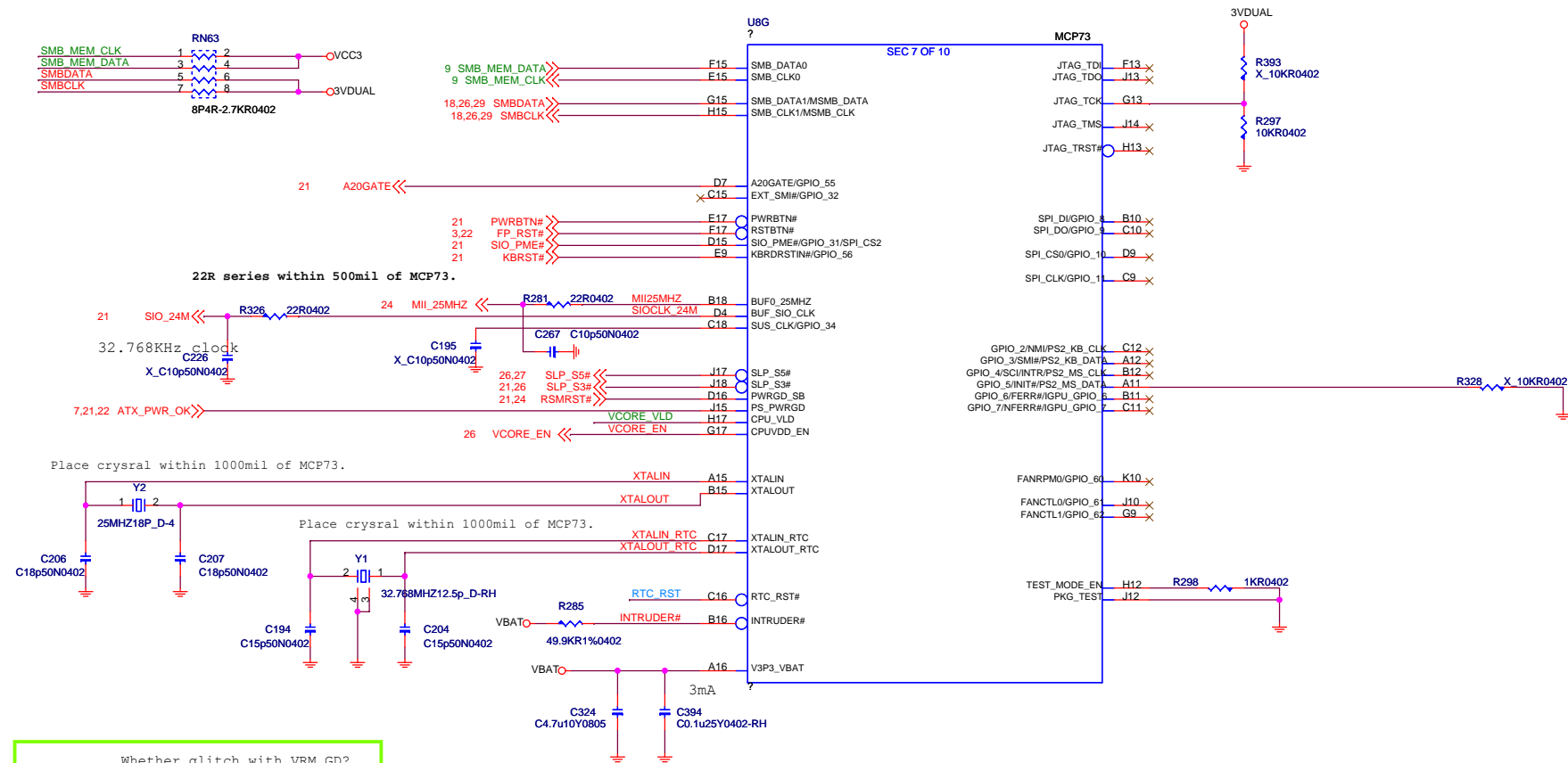
Size	Document Description	Rev
Custom	MCP73-SATA/IDE	0A
Date: Monday, October 15, 2007	Sheet 12 of 38	

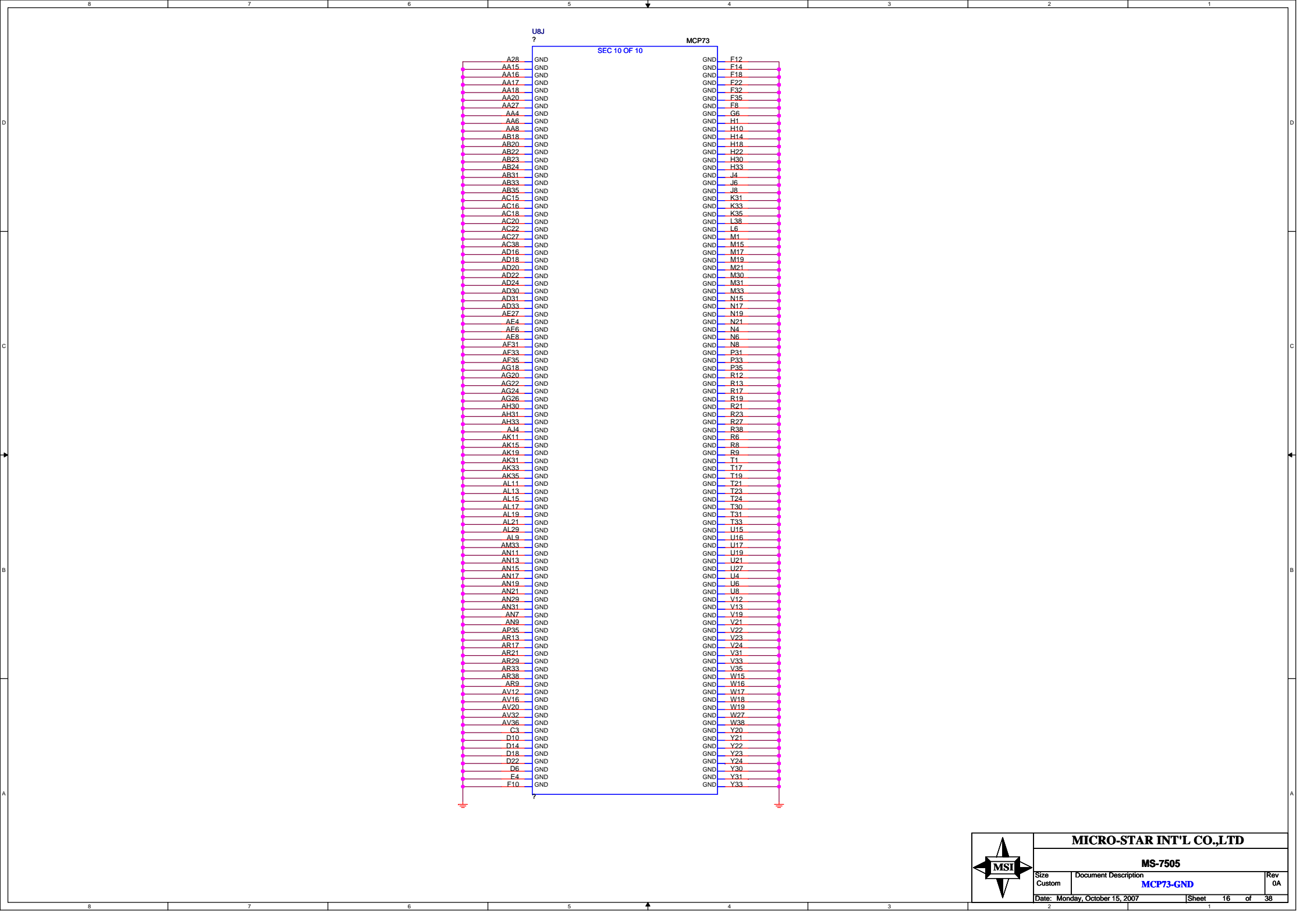


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Size	Document Description	Rev
Custom	MCP51-Audio/USB/GPIO	0A
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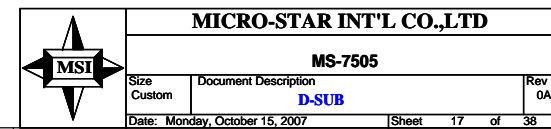


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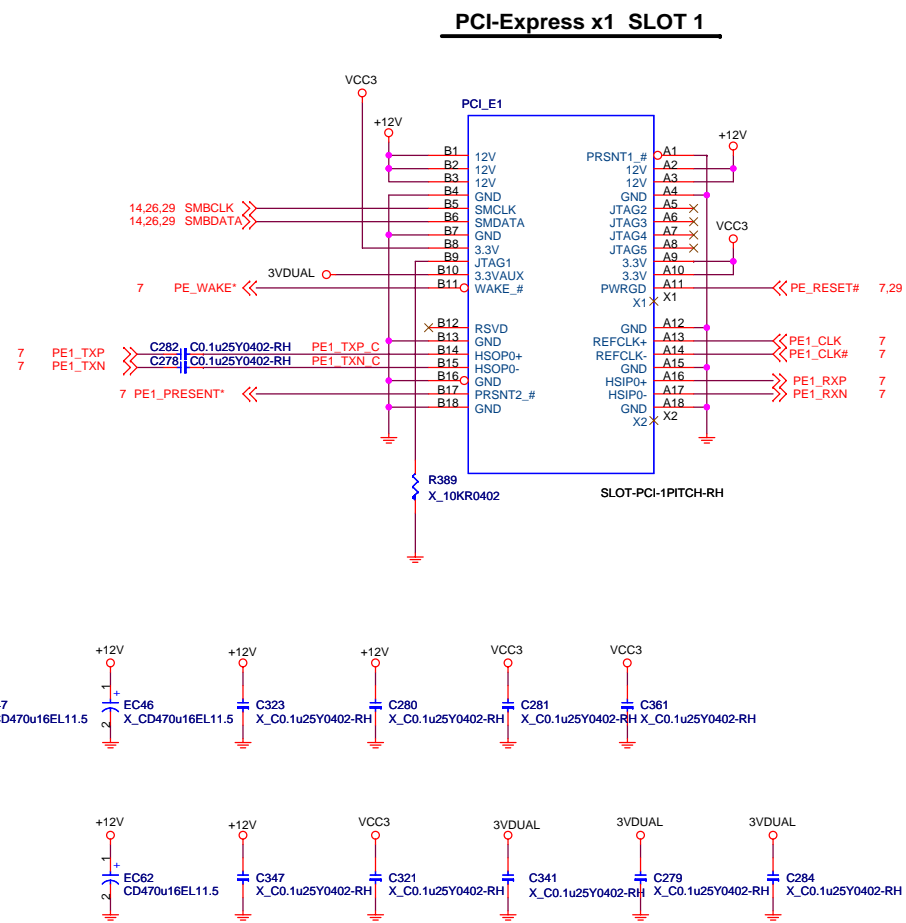
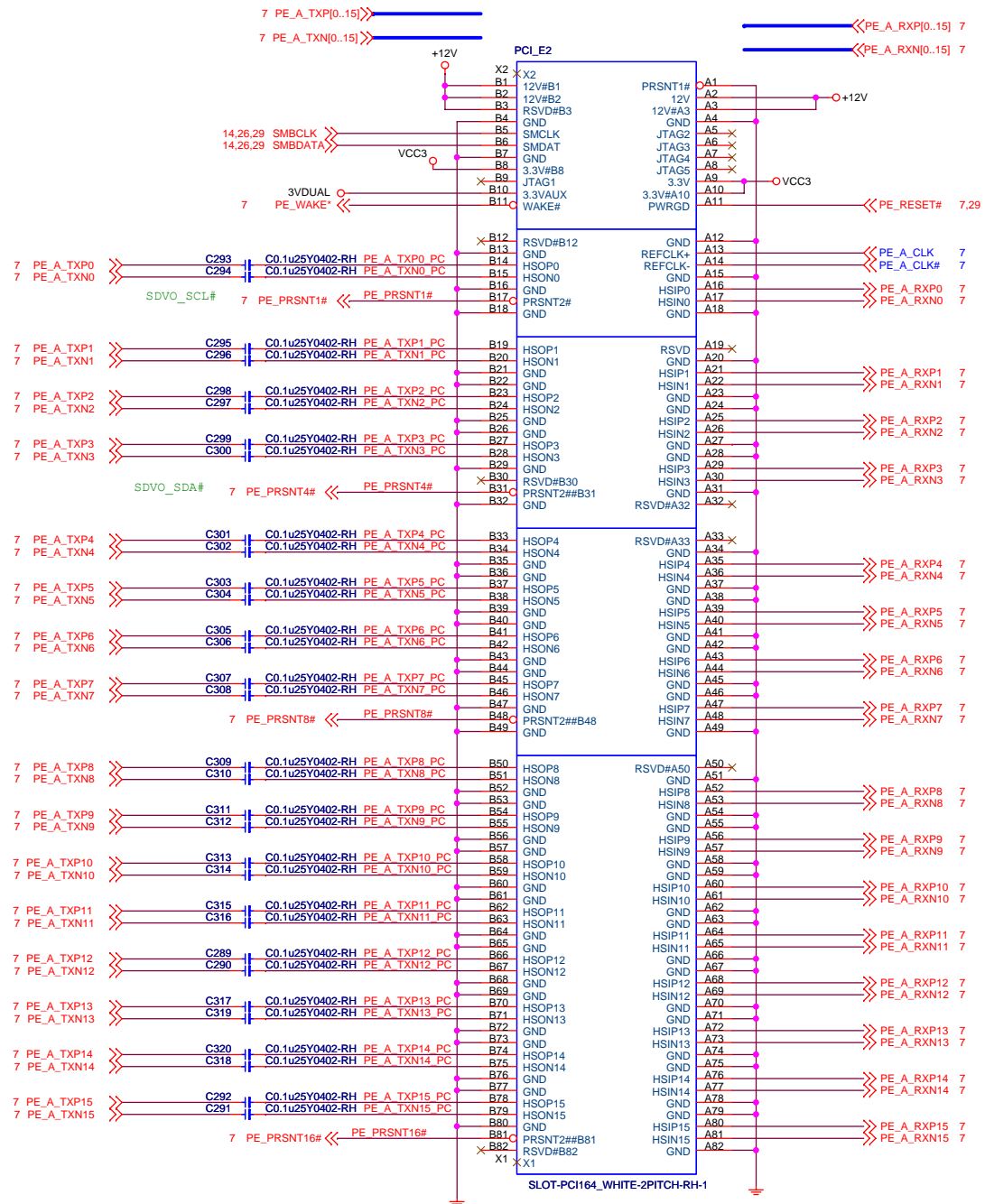
MS-7505

Size	Document Description	Rev
Custom	MCP73-GND	0A
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```
7 DDC_CLK >
```



PCI-Express X16 Primary Slot X16/X8

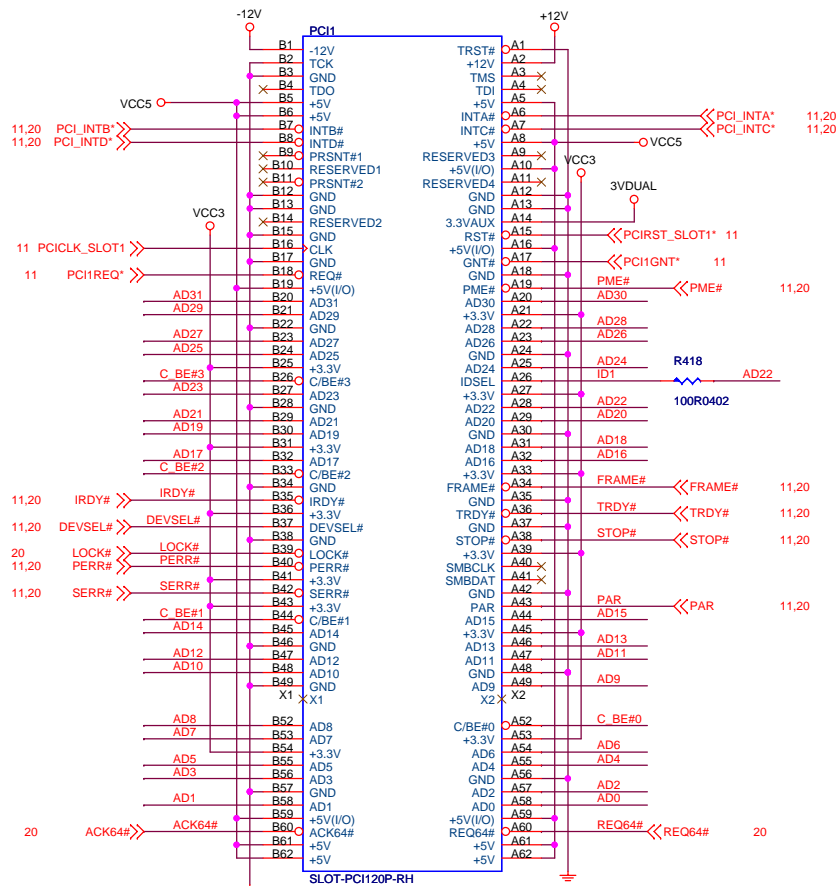


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Size Custom	Document Description PCI-E X16/X1 Slot	Rev 0A
Date: Monday, October 15, 2007		Sheet 18 of 36

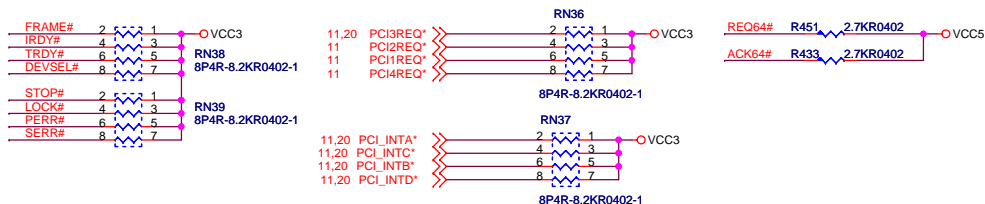
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



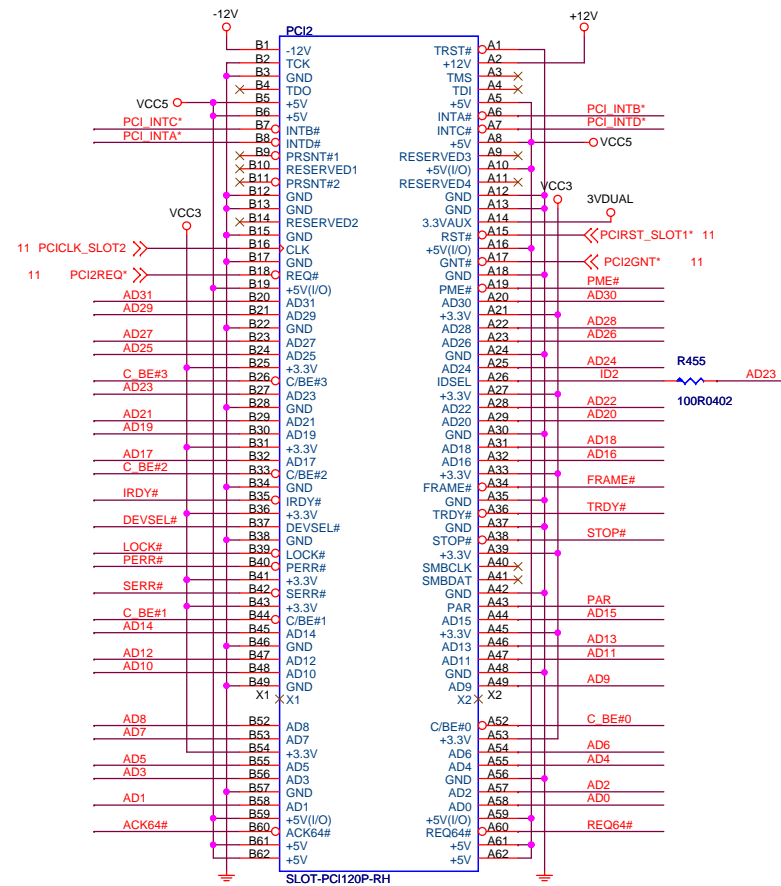
IDSEL = AD22
MASTER = PCI1REQ*
PCI1GNT*

11,20 AD[31..0] >> AD[31..0]
11,20 C_BE#[3..0] >> C_BE#[3..0]

PCI PULL-UP / DOWN RESISTORS



PCI SLOT 2 (PCI VER: 2.2 COMPLY)



IDSEL = AD23
MASTER = PCI2REQ*
PCI2GNT*

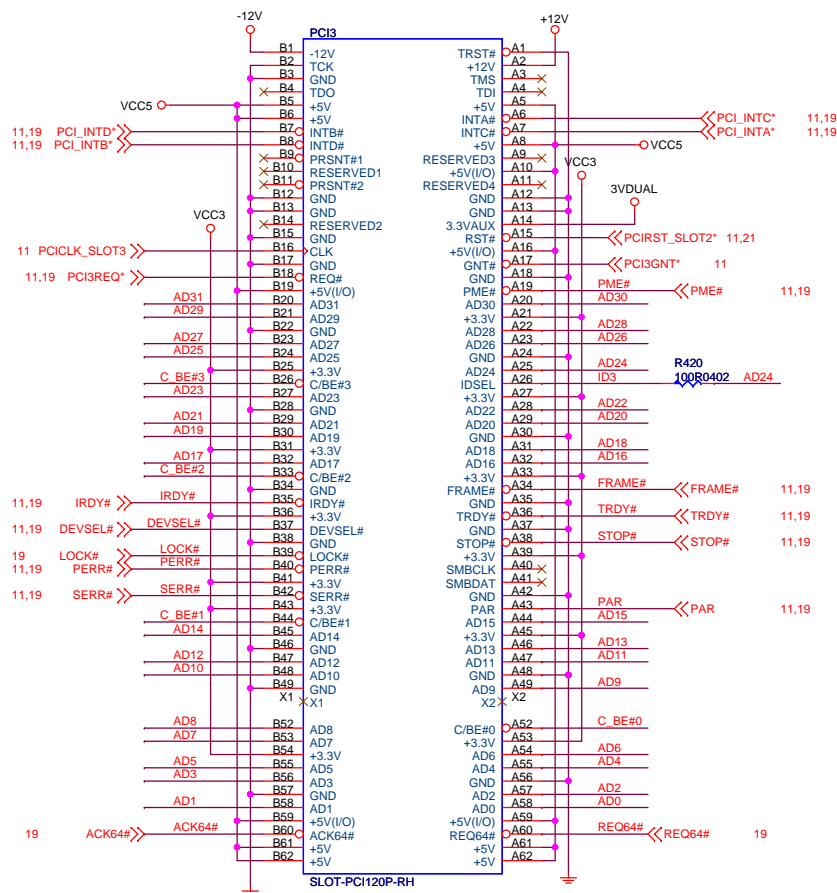


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Size	Document Description	Rev
Custom	PCI Slot 1 & 2 & 3	0A
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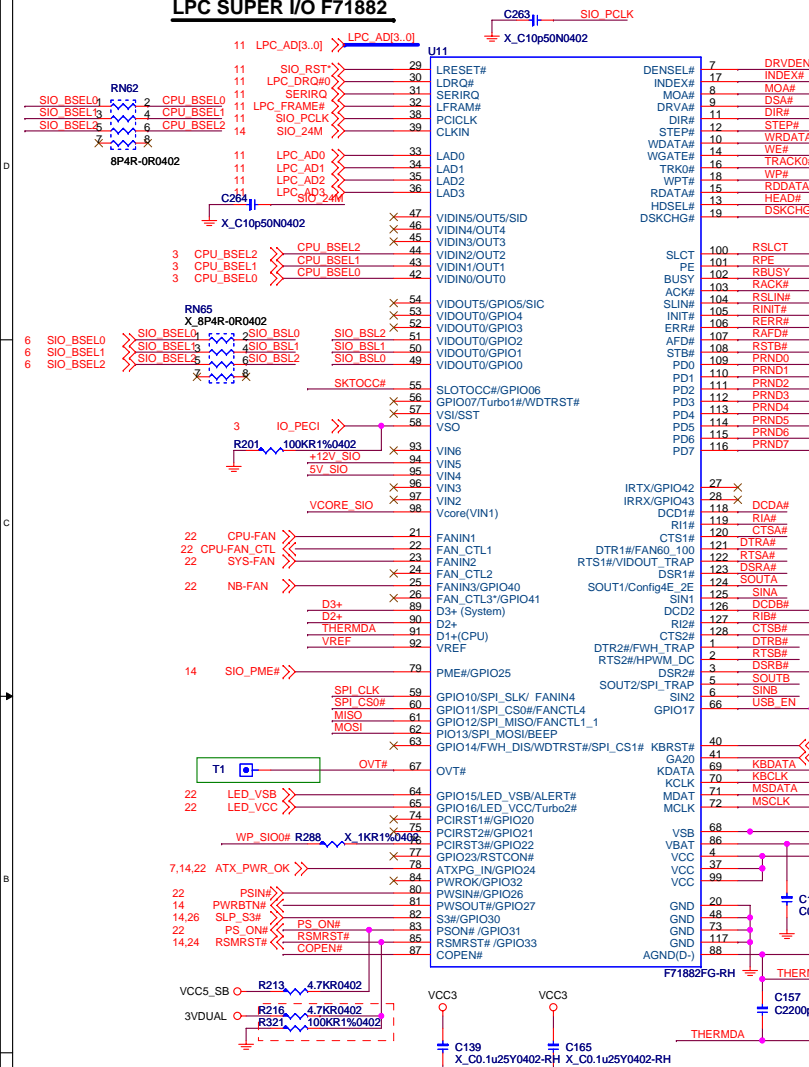
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



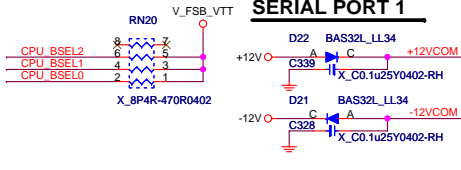
IDSEL = AD24
 MASTER = PCI3REQ*
 PCI3GNT*

11,19 AD[31..0] >> AD[31..0]
 11,19 C_BE#[3..0] >> C_BE#[3..0]

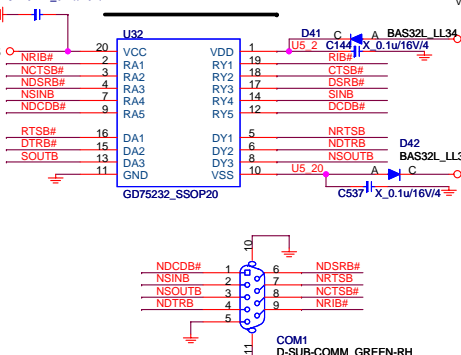
LPC SUPER I/O F71882



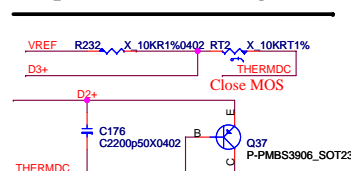
SERIAL PORT 1



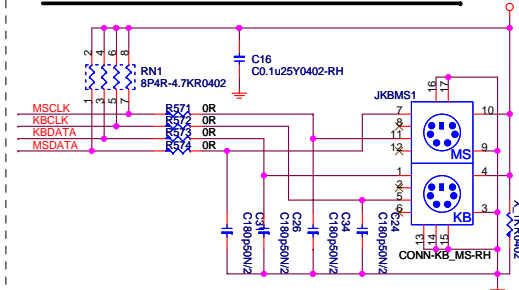
SERIAL PORT 2



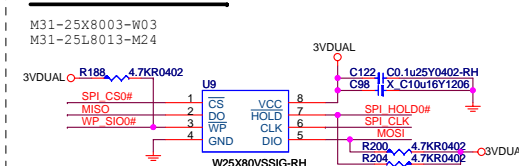
Temperature Sensing (HWM)



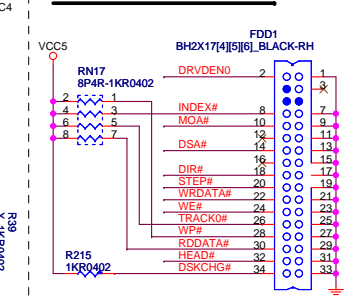
PS2 KEYBOARD & MOUSE CONNECTOR



SPI 8M FLASH ROM



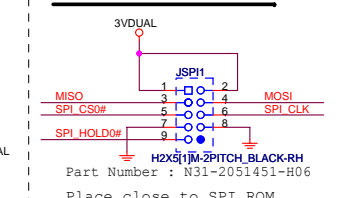
FLOPPY Connector



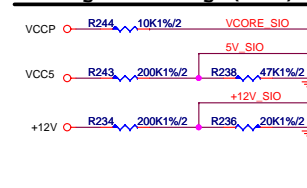
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SPI DEBUG PORT

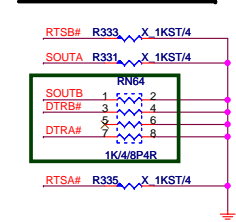
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Voltage Sensing (HWM).

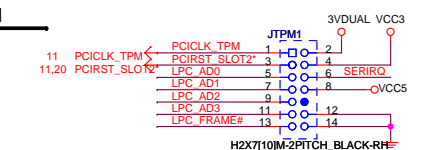


Strapping



Pin #	Pin Name	Description
Pin 1	DTKB#	1-SPI as a Backup BIOS (Default) 0-SPI as a Primary BIOS
Pin 2	RTSB#	1-Fan Control Mode : PWM Mode.(Default) 0-Fan Control Mode : Linear Mode.
Pin 5	SOUTH	1-SPI Function Disable. (Default) 0-SPI Function Enable.
Pin 121	DTRA#	1-Power On Fan speed as 60% duty(PWM) (Default) 0-Power On Fan with Full speed. (PWM)
Pin 122	RTSA#	1-6 Pins VIDI# and 6 Pins VIDO#(Default) 0-VIDI#OUT on 6 pins, VIDO# Pin will be GPIO
Pin 124	SOUTA	1-Config. Register I/O Port is 4E/4F.(Default) 0-Config. Register I/O Port is 2E/2F.

JTPM



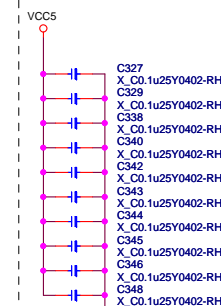
MICRO-STAR INT'L CO.,LTD

MS-7505

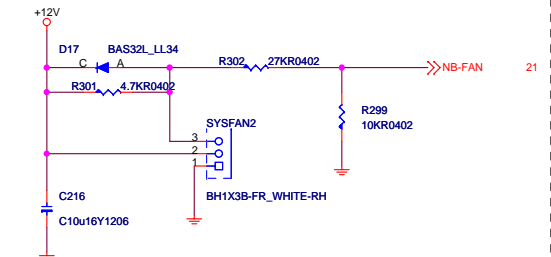
LPC-Super I/O F71882FG

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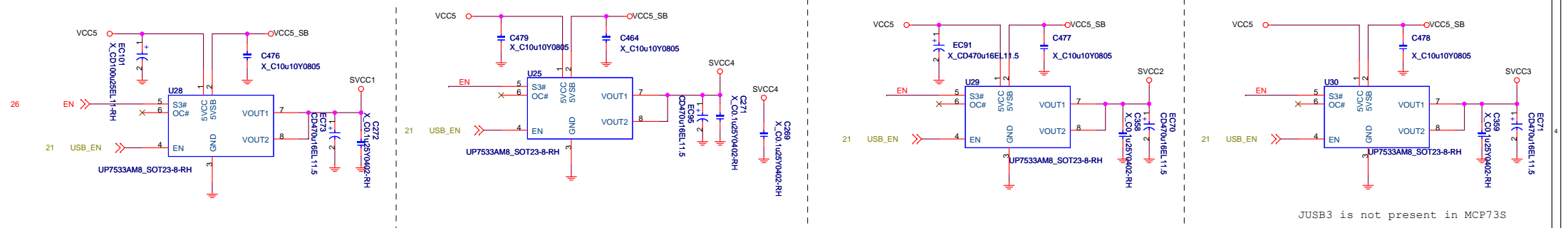
Intel Front Panel



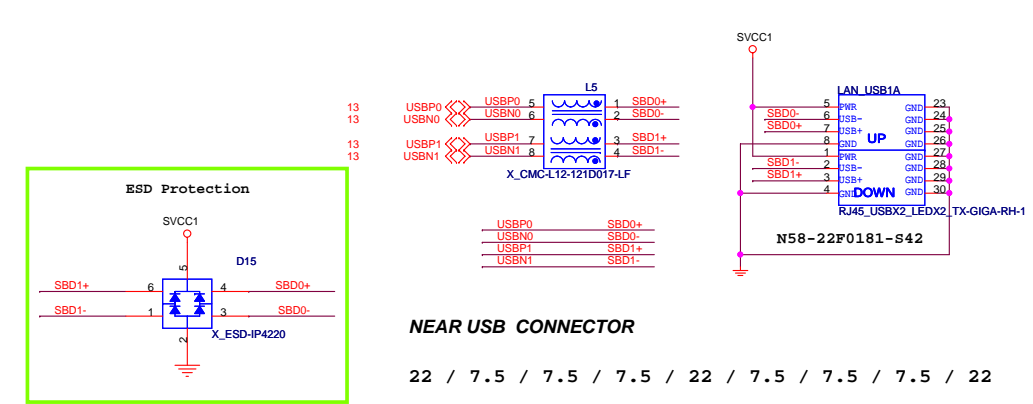
Reserve for NB_FAN, Near MCP73
MP Remove

**MS-7505**

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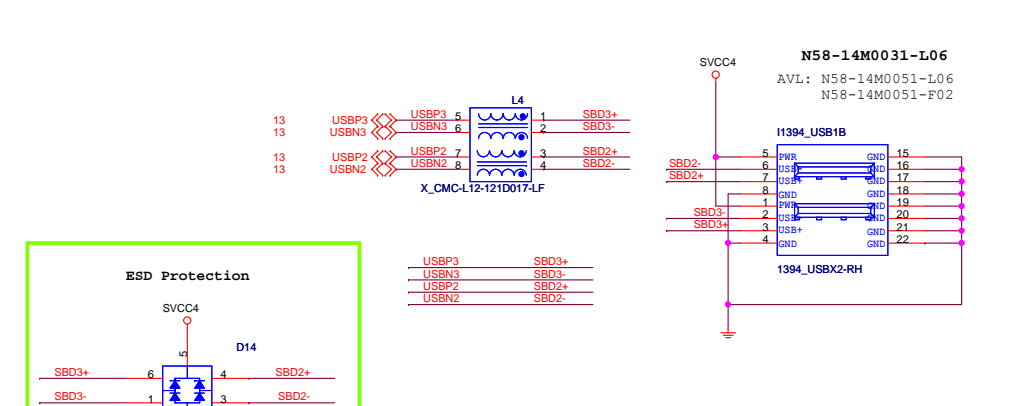
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

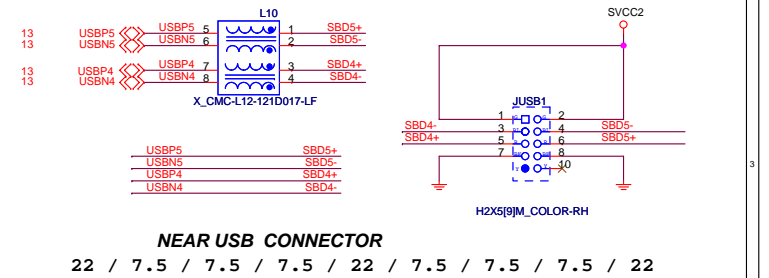
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

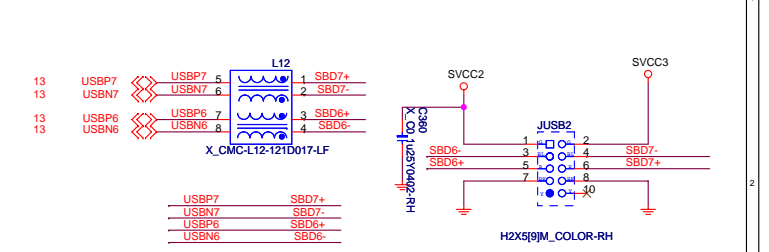
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



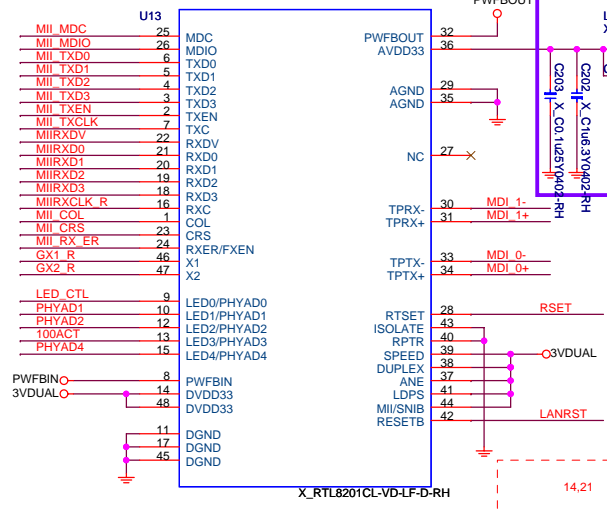
NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

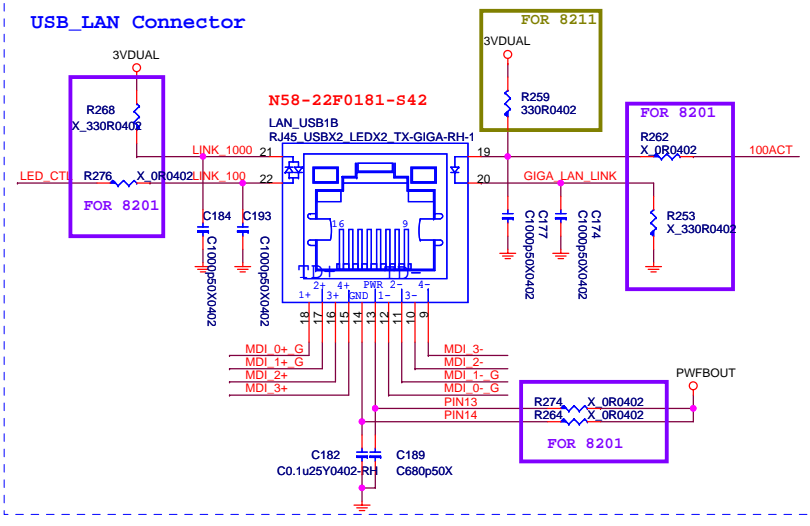
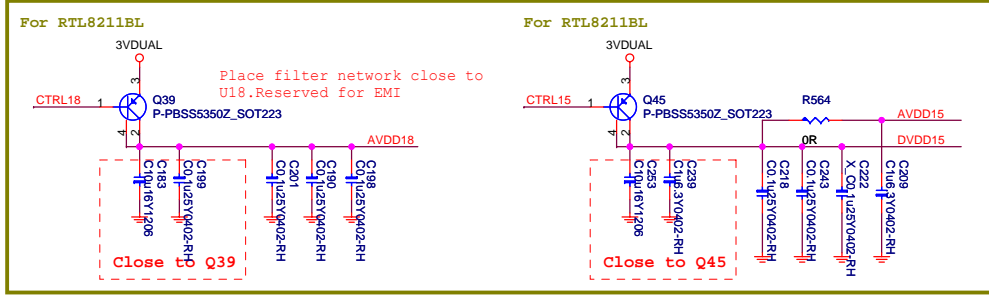
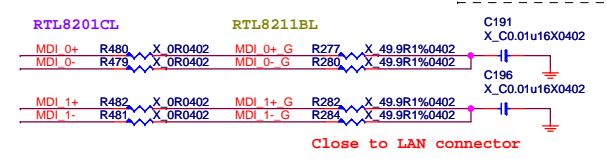
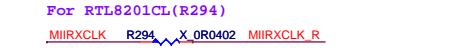
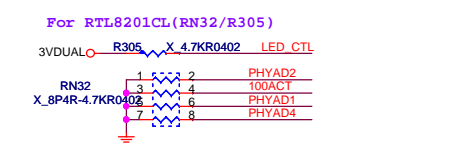
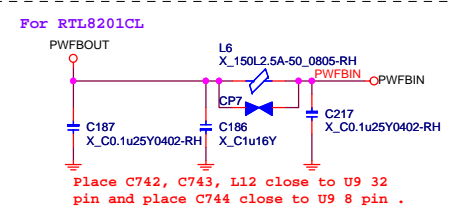
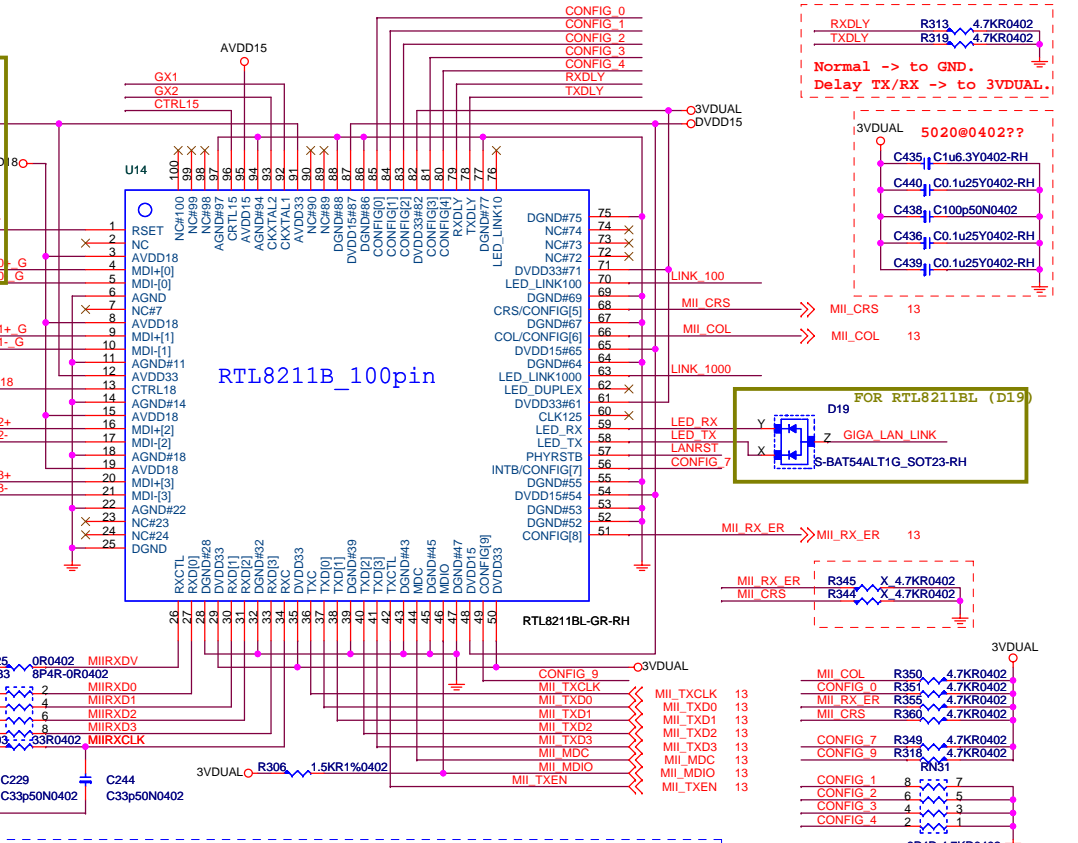
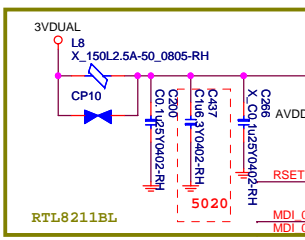
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7






RTL8201CL

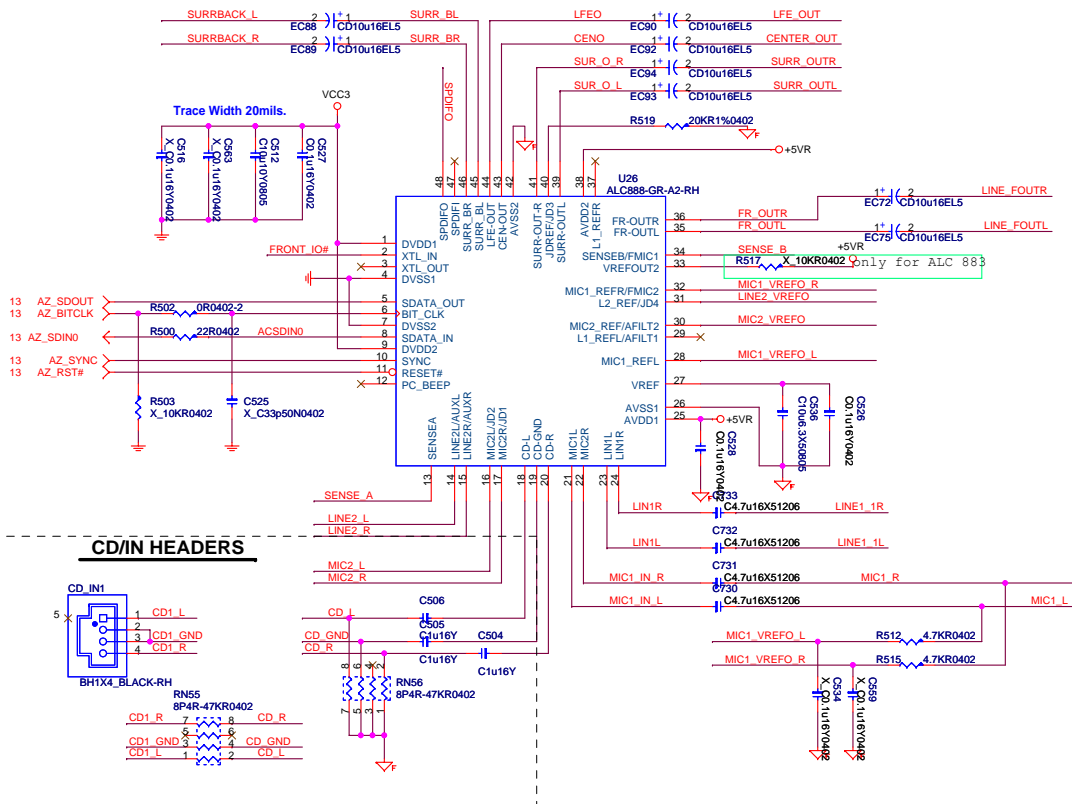


RTL8211BL

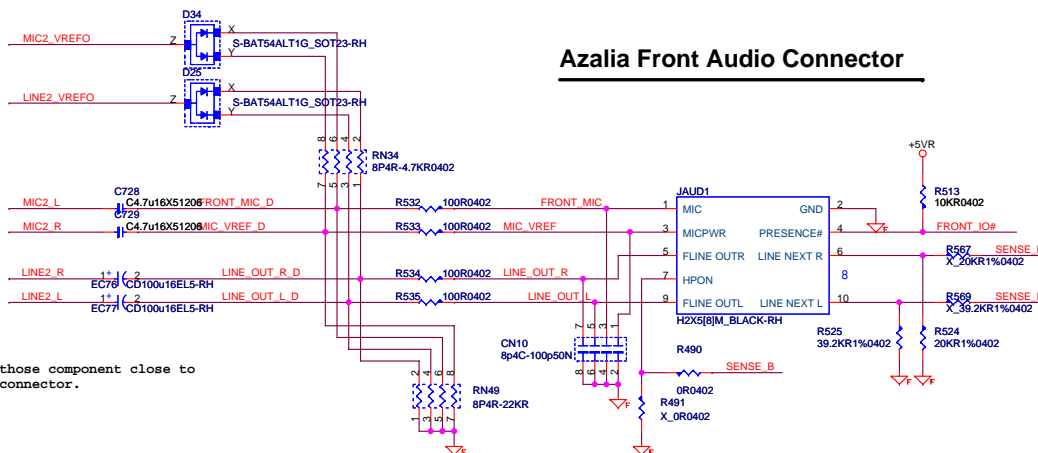


Giga-Lan		10/100-Lan	
N58-22F0181-S42		N58-22F0201-S42 N58-22F0341-S42 N58-22F0281-F02	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20	Yellow	20	Yellow
21	Orange	21	
22	Green	22	Green

ALC888 CODEC

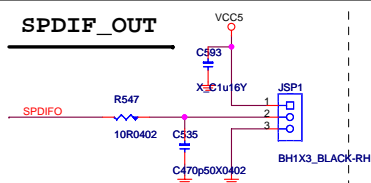


Azalia Front Audio Connector

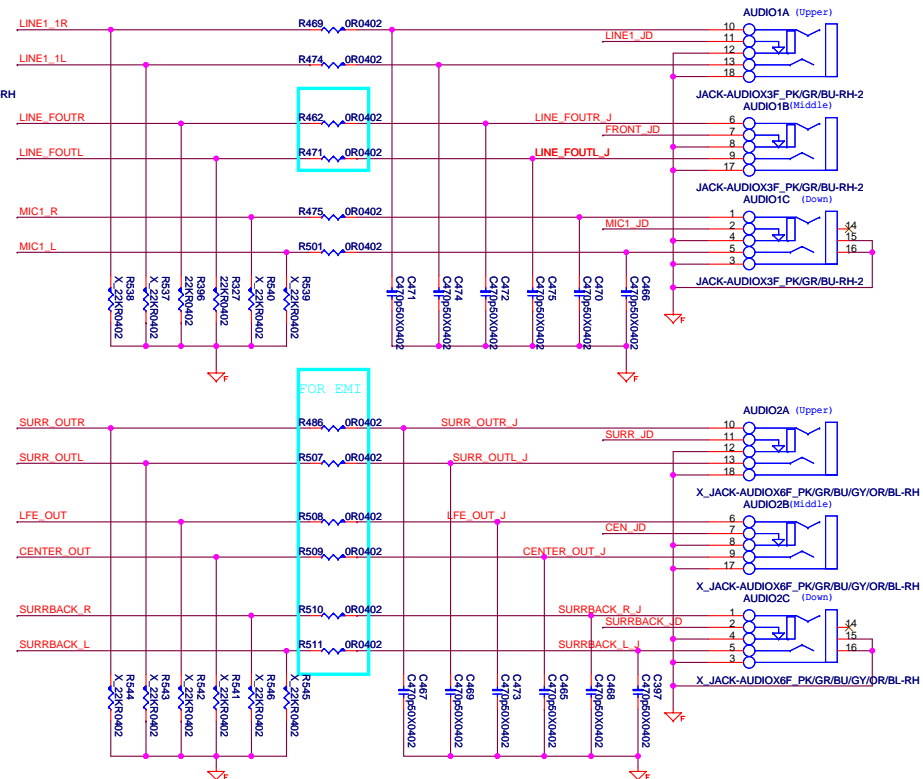


Place those component close to
audio connector.

SPDIF_OUT



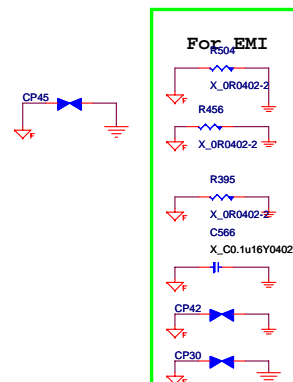
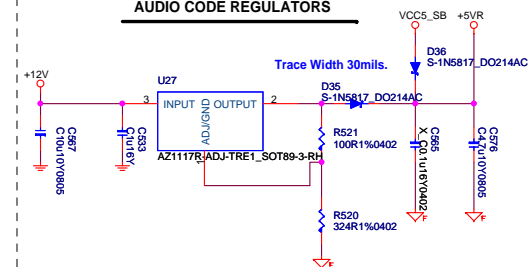
ALC883 JACK



ALC883 JACK DETECT

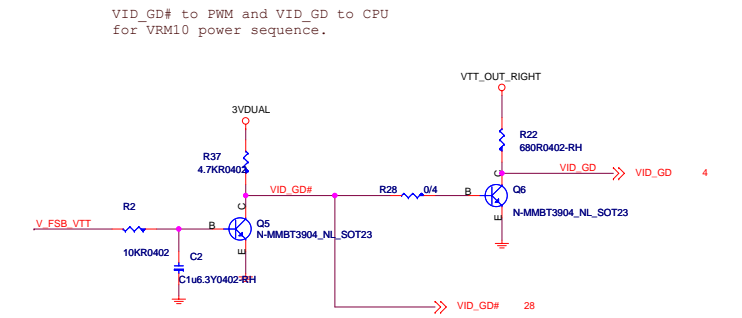
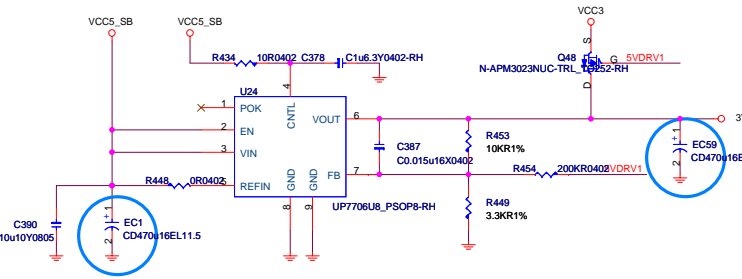
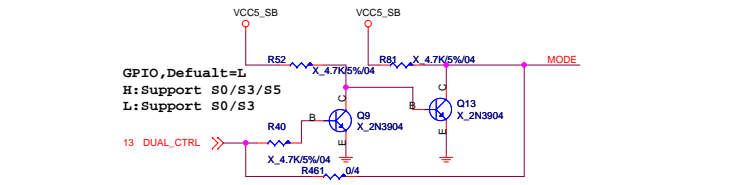
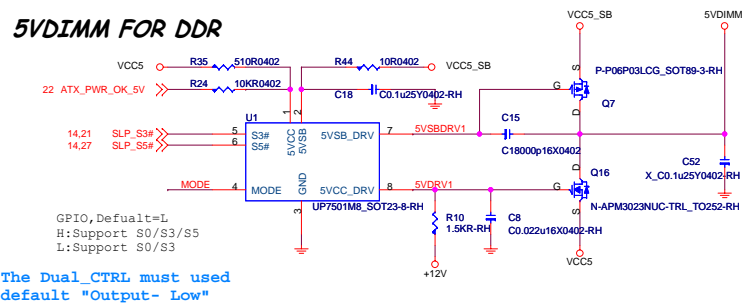


AUDIO CODE REGULATORS



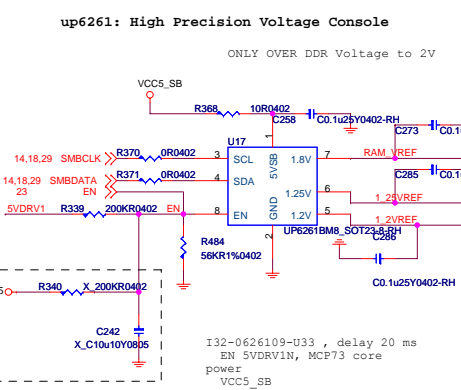
MICRO-STAR INT'L CO.,LTD			
MS-7505			
Size Custom	Document Description Azalia CODEC(ALC888&alc883)		Rev 0
Date: Tuesday, October 16, 2007		Sheet 25	of 36

5VDIMM FOR DDR



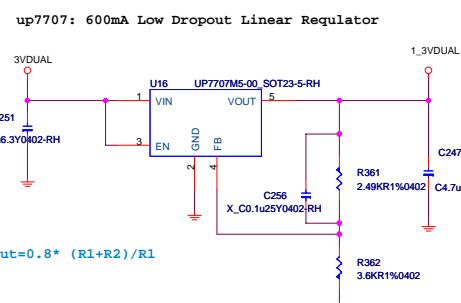
	S0	S3	S4	S5
DUAL_CTRL	X	X	0	1
5VSBDRV1	1	0	1	0
5VDRV1	1	0	0	0
5VSBDRV2	X	0	1	0
USB_MODE	X	1	X	1
5VDIMM	Y	Y	N	Y
USB power	Y	Y	N	Y

Reference Voltage



EN : 0.4~1.4V

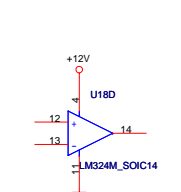
1_3VDUAL, 25mA



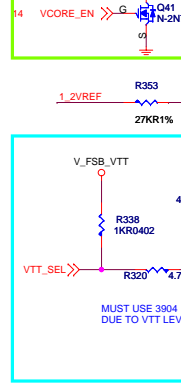
VCC1_5, 8.81A 2.643W

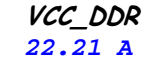
I71-LM32403-T07
I71-LM32413-Q05
I71-LM32413-F01
I71-LM32413-N04

VCC1_3, 8.81A 1.32W



FSB_VTT, 6.1A 3.66W

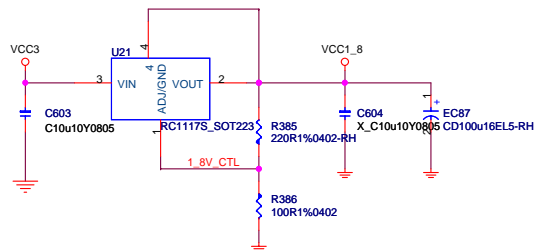
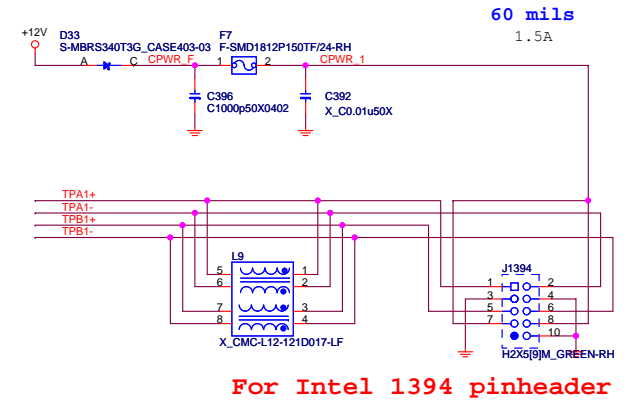
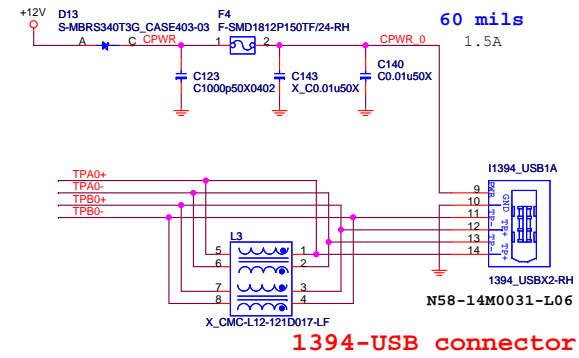
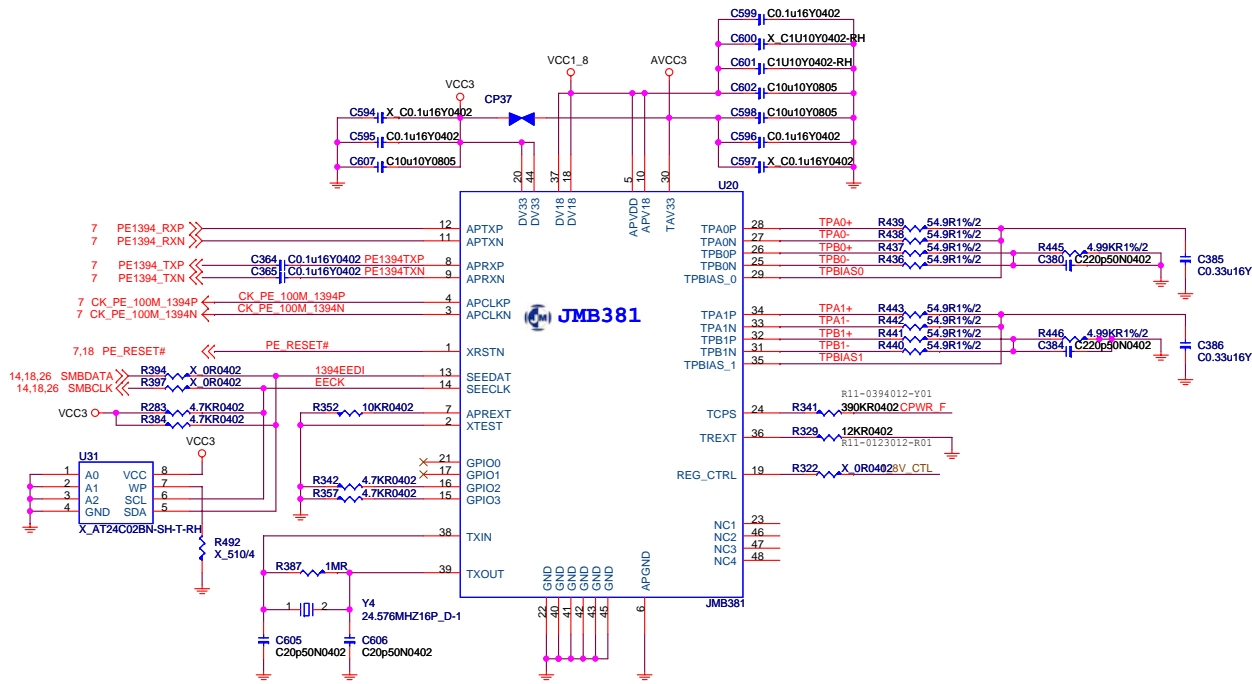


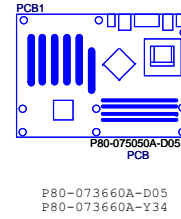
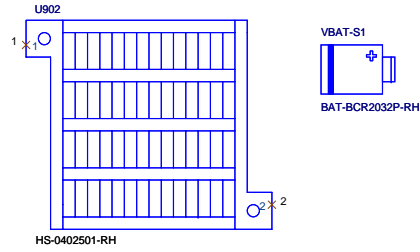
$$I_{ripple} = 22.21 \times 0.6 \times 0.8 / 1 = 10.66A$$
$$2.35 \times 3 \times 1.7 = 11.985A > 10.08A$$


To CPU Copper trace width > 200mils

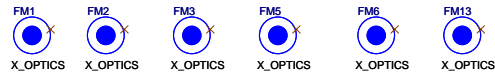




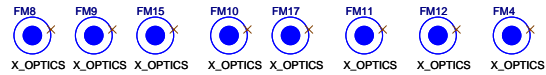




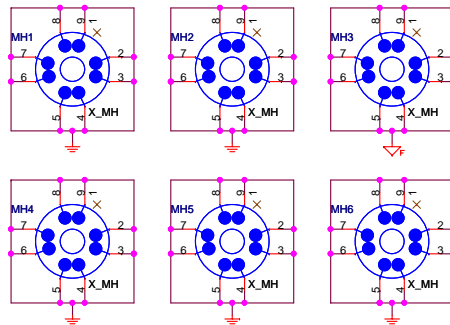
Optics Orientation Holes (F_PAD_M100)



Optics Orientation Holes (F_PAD_M120)



Mounting Holes



Simulation

